



Reliability Report

Report Title: LTM4705 Material Set Change Qualification

Report Number: 22621

Revision: A

Date: 4 December 2024

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the material set change of the LTM4705 product in a 63-CSP_BGA package. The LTM4705 is 20VIN, Dual 5A or Single 10A Step-Down DC/DC μ Module Regulator. The only change made is the die thickness from 450um to 200um.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	LTM4705
Die Id	3636
Die Size (mm)	2.29 x 3.35
Wafer Fabrication Site	TSMC
Wafer Fabrication Process	0.35um BCDMOS
Die Substrate	Si
Metallization / # Layers	AlCu/4
Polyimide	No
Passivation	oxide/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results - 0.35um BCDMOS at TSMC

Test Name	Specification	Conditions	Device	Lot #	Fail/SS
High Temperature Storage Life (HTSL)	JESD22-A103	+150°C, 1,000 hours	LTM4705	Q17764.1HTS	0/45
				Q17764.2HTS	0/45
				Q17764.3HTS	0/45
Highly Accelerated Temperature and Humidity Stress Test (HAST) ¹	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264 Hours	LTM4705	Q17764.1BHAST	0/25
				Q17764.1BHAST-REPLACE	0/25
				Q17764.3RESUB.RCM BHAST	0/25
High Temperature Operating Life (HTOL)	JESD22-A108	Ta = 125C, Biased, 1000 hours	LTM4705	Q17764.1HTOL	0/77
				Q17764.2HTOL	0/77
				Q17764.3HTOL	0/77
Power Cycle	06-04-0012	Tj=25°C to 80°C, Biased, 50,000 Cycles.	LTM4705	Q17764.1PWRCYC	0/8
				Q17764.2PWRCYC	0/8
				Q17764.3PWRCYC	0/8

¹ These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 48 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 250°C.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 63-CSP_BGA at ASE Korea

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	LTM4705
Package	63-CSP_BGA
Body Size (mm)	7.50 x 6.25 x 3.22
Assembly Location	ASE Korea
MSL/Peak Reflow Temperature(°C)	3 / 250°C
Mold Compound	Sumitomo G311E
Substrate Material	BT Resin
Solder Ball Composition	96.5Sn_3.0Ag_0.5Cu
Solder Ball Size (mm)	0.50

Package/Assembly Test Results

Table 4: Package/Assembly Test Results - CSP_BGA at ASE Korea

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Solder Heat Resistance (SHR)	J-STD-020	MSL-3	LTM4705	Q22621.1.MSL3 ²	0/231
Temperature Cycling (TC) ¹	JESD22-A104	-55°C /+125°C, 1,000 Cycles	LTM4705	Q22621.1.TC3 ²	0/77
				Q17764.1TC	0/77
				Q17764.1TC-REPLACE	0/77
				Q17764.3TC	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST) ¹	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264 Hours	LTM4705	Q17764.1BHAST	0/25
				Q17764.1BHAST-REPLACE	0/25
				Q17764.3RESUB.RCMBHAST	0/25
Unbiased HAST (UHAST) ¹	JESD22-A118	110C 85%RH 17.7 psia, 264 Hours	LTM4705	Q17764.1UHAST	0/77
				Q17764.1UHAST-REPLACE	0/77
				Q17764.3UHAST	0/77

¹ These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 48 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 250°C.

² Stress test with 200µm die.

Note: J-STD-020 rework compatibility was verified passing by performing Bake: 48 hrs @ 125°C, Unbiased Soak: 8 hrs @ 30°C, 60%RH, Reflow: 1 pass through a reflow oven with a peak temperature of 260°C.

ESD and Latch-Up Test Results

Table 5: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	LTM4705	63-CSP_BGA	JS-002	1Ω, Cpkg	±1250V	C3
HBM	LTM4705	63-CSP_BGA	JS-001	1.5kΩ, 100pF	±4000V	3A

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T _A)	Class
JESD78	LTM4705 ¹	+200mA, -200mA	+27/4.5V	25°C	I

¹ Stress test with 200μm die.

Approvals

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